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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,177	11/03/2003	Mukesh K. Puri	03-0291	3593

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/700,177	PURI ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to the Amendment filed 7/15/2008.

Claims 1-18 were rejected in the prior Office Action.

Claim 2 is cancelled. Claims 1 and 3-18 are pending.

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings Fig. 1-3 are informal. Formal drawings may be submitted upon Allowance of the Application.

Rejection of the Claims under 35 U.S.C. 112, second paragraph, has been withdrawn in view of the amendment to the claims.

Response to Arguments

Applicant's arguments filed 7/15/2008 with respect to claims 1-18 have been fully considered but they are not persuasive.

Applicant argues that Zorian neither discloses nor suggests the limitations recited in the independent claims 1 and 12, as currently amended, which now specifically claims "loading a value into an on-chip counter through a test pattern during production testing, where the value represents an amount of redundant elements which are allowed for a repair....., using a repair solution to repair a first set of damaged memories while not repairing and instead flagging a second set of damaged memories, wherein each of the memories in the second set have been determined to require a number of redundant elements to be used for the repair, where the number exceeds the value which has been loaded into the on-chip counter".

In response to Applicant's argument that Zorian fails to disclose the above new limitations, the Examiner wishes to direct Applicant's attention to Zorian, Fig. 8, showing a Built-In Redundancy Analysis (BIRA) engine 802 that determines whether a memory array will be repairable or not repairable, based on the assignment of redundant rows or columns, where the (BIRA) engine 802 allocates the redundant components, such as one or more redundant columns and the one or more redundant rows. In this case for the sake or argument, the repairable feature corresponds to the claimed limitation "a first set of damaged memories", the not repairable feature corresponds to the claimed limitation "a second set of damaged memories", and the status bit registers 810 and 812

corresponds to the claimed limitation of "loading a value into an on-chip counter, where the value represents an amount of redundant elements which are allowed for a repair". The status bit registers 810 and 812 record the status of redundant row registers, and indicate whether the corresponding redundant row is available or unavailable as a substitute row. Similarly, status bit register-CL (not shown) and status bit register-CH (not shown) record the status of redundant column registers. The status bit registers indicate whether the corresponding redundant column is available or unavailable as a substitute column.

The BIRA engine 802 assigns the redundant components determines whether a memory array will be repairable or not repairable, thereby, increasing or decreasing the yield of useable memories on the chip. According to a first Built-In -Redundancy-Analysis algorithm:

First, if at least two faulty cells are encountered, then the row requires repair with a redundant row. If an available redundant row does not exist, then the memory array is considered unrepairable.

Second, if a single faulty cell is encountered, then a redundant column is used for repair, if available. If no spare column is available but a spare row is available, then a redundant row is used for repair. Otherwise, the memory array is considered unrepairable.

Therefore, the limitation "flagging a second set of damaged memories" corresponds to not repairable memory array feature, since the failed memory array requires extensive repair.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Zorian (US 7,237,154) filed: February 25, 2002.

Regarding independent Claims 1, 12, Zorian discloses a method and apparatus that generate an augmented repair signature to repair all of the defects detected in a first test of a memory as well as in a second test of the memory, comprising:

Testing the memories a first time; "A first test of the memory occurs and a first redundancy allocation algorithm 232 is run. The redundancy allocation algorithm identifies defects and then allocates redundant components to replace those identified defects", Fig. 2b.

Generating a repair solution; "The reconfiguration logic collects data from the results of the redundancy allocation algorithm to generate a first repair signature 234. The first test and/or the repair algorithms may be performed by logic on the chip or by test equipment external to the chip".

Using the repair solution (first repair signature 234) to repair the memories while flagging those memories whose repair exceeds a pre-determined limit; "The repair signature (234) includes a coded sequence to allocate redundant components to substitute for defective components in order to make the memory usable. The coded sequence loads into registers associated with the redundancy allocation logic to replace all of the identified defective components with redundant components".

Making an on-chip assessment to test the memories a second time; "A quality assurance built in self-test 236 runs to determine that all defects in the memory have been eliminated through the use of redundant components and that the assigned redundant components have no defects".

Using the repair solution (234) to repair the memories not previously flagged; "The configuration logic in the processor may receive the existing first repair signature 234 from a storage device external to the chip or from the fuse box. When the reconfiguration logic receives the first repair signature 234, the reconfiguration logic may initiate a second test algorithm and second redundancy allocation algorithm 238 to attempt to repair the memory. The test logic provides the results of the second test, thus all known and identified defects, to the redundancy algorithm to repair all of the defects in the memory. The reconfiguration logic then generates a second repair signature 240. After the redundancy allocation logic assigns the corresponding redundant components to replace identified defective components, then a quality assurance built in self test of the memory 236 runs one more time just to make sure that the redundant components substituted for the defective components, also do not have defects".

Also, as shown in Fig. 3, the BIRA engine 308 (Built-in Redundancy Allocation) identifies and allocates available redundant rows and redundant columns in order to determine the optimum redundancy scheme when a failure occurs. Also, Fig. 4 shows available redundancy 404, which corresponds to "loading a value into an on-chip counter through a test pattern during production testing, where the value represents an amount of redundant elements which are allowed for a repair".

Regarding Claims 3-11, 13-18, Zorian discloses, with respect to claimed limitation of loading a counter with values to establish a threshold for pass/fail criteria, Built-In Redundancy Analysis (BIRA) engine 802, Figs. 8, having a plurality of registers for allocating redundant columns and rows. The registers (804) store information for final self-repair. If the memory is diagnosed as repairable the final contents of the registers contain the addresses of rows and columns to be replaced with the corresponding spare elements. The BIRA engine 802 determines whether a memory array will be repairable or not repairable, based on the assignment of redundant rows or columns.

If at least two faulty cells are encountered in a word either in the lower bank or the upper bank of the memory array, then the row requires repair with a redundant row. If an available redundant row does not exist, then the memory array is considered not repairable.

If a single faulty cell is encountered in a word either in the lower bank or the upper bank of the memory array then a redundant column is used for repair, if available.

If no spare column is available but a spare row is available, then a redundant row is used for repair. Otherwise, the memory array is considered not repairable.

In this case, the pre-determined limit corresponds to the number of spare rows or columns, where the pre-determined limit is used as a criterion to determine whether a memory array is repairable or not repairable, as described previously.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 8 September 2008
Office Action: Final Rejection

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